

TITLE OF THE INVENTION

APPARATUS AND METHOD GENERATING ERROR FLAG FOR ERROR CORRECTION

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of Korean Patent Application No. 2003-11637, filed on February 25, 2003, in the Korean Intellectual Property Office, the disclosure of which is incorporated herein by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0002] The present invention relates to an apparatus and method generating an error flag for error correction.

2. Description of the Related Art

[0003] To store information in an optical recording medium such as CD or DVD, error-correction coding (ECC) is performed in which parity data is added to user data to generate a codeword and the codeword is processed according to a predetermined method. If the user data is 30 bytes, the parity data is 30 bytes, and accordingly one codeword is 60 bytes, error correction is possible although errors are generated in maximal 15 bytes of one codeword when decoding is performed. However, if an error flag indicating the location of data including an error in the codeword is provided, error correction is possible although errors are generated in maximal 30 bytes of the codeword.

[0004] Such a technique that improves error correction performance using an error flag is called erasure correction. The erasure correction has higher error correction efficiency where a burst error is generated rather than a random error.

[0005] U.S. Patent No. 6,367,049 discloses an error correction format consisting of a plurality of ECC (Error Correction Code) columns and a plurality of BIS (Burst Indicator Subcode)

columns. BIS is information that is inserted when decoding is performed, in order to indicate the generation of a burst error. A reliability of a decoded BIS is higher than that of ECC.

[0006] FIG. 1 is a view showing a data block with an error correction format disclosed in the above-described U.S. Patent No. 6,367,049.

[0007] According to the error correction format, in one data block, frame synchronization (frame-sync) data is included in the heading of the data block, and subsequently 38 ECC columns and one BIS column are located alternately. One data block has 496 frames. Data constructing the data block is interleaved according to a predetermined method. The detailed descriptions related to the error correction format and interleaving are disclosed in the above-described U.S. Patent Application No. 6,367,049.

[0008] FIG. 2 shows a detailed structure of one frame forming part of the data block of FIG. 1.

[0009] Referring to FIG. 2, in one frame, frame-sync data is included in the heading of the frame and subsequently 38-byte ECC and one-byte BIS are located alternately.

[0010] However, an error correction system according to the error correction format shown in FIGS. 1 and 2 has problems in that an interleaving process is complex, accordingly the generation of an error flag for erasure correction is not easy, and a hardware structure is complicated.

SUMMARY OF THE INVENTION

[0011] The present invention provides an apparatus and method generating an error flag for error correction, having improved performance and being advantageous in cost.

[0012] According to an aspect of the present invention, there is provided an apparatus generating an error flag, the apparatus including: a frame-sync error memory which stores frame-sync error information for each data block; a BIS (Burst Indicator Subcode) error flag memory which stores a BIS error flag for each data block; and an error flag generator, which generates an error flag indicating error existence/absence for ECC (Error-Correction Coding) data with reference to the frame-sync error information stored in the frame-sync error memory and the BIS error flag stored in the BIS error flag memory.

[0013] According to another aspect of the present invention, there is provided an error flag generation method comprising: receiving a reproduced digital signal; generating frame-sync error information for each data block using the reproduced digital signal; storing the frame-sync error information in a frame-sync error memory for each data block; generating a BIS error flag of the data block for each data block; storing the BIS error flag of the data block in a BIS error flag memory for each data block; and generating an error flag indicating error existence/absence for ECC data with reference to the frame-sync error information stored in the frame-sync error memory and the BIS error flag stored in the BIS error flag memory.

[0014] Additional aspects and/or advantages of the invention will be set forth in part in the description which follows and, in part, will be obvious from the description, or may be learned by practice of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] These and/or other aspects and advantages of the invention will become apparent and more readily appreciated from the following description of the embodiments, taken in conjunction with the accompanying drawings of which:

FIG. 1 is a view showing a data block with an error correction format according to a conventional technique;

FIG. 2 shows a detailed structure of one frame forming part of the data block of FIG. 1;

FIG. 3 is a block diagram of an apparatus for generating an error flag, according to an embodiment of the present invention;

FIGS. 4A-4C are timing charts describing the generation of a frame synchronization (frame-sync) error signal;

FIG. 5 is a view showing a structure of a frame synchronization (frame-sync) error memory of FIG. 3;

FIG. 6 is a view showing a structure of a BIS (Burst Indicator Subcode) error flag memory of FIG. 3; and

FIG. 7 is a flowchart illustrating a method for generating an error flag, according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0016] Reference will now be made in detail to the embodiments of the present invention, examples of which are illustrated in the accompanying drawings, wherein like reference numerals refer to the like elements throughout. The embodiments are described below to explain the present invention by referring to the figures.

[0017] FIG. 3 is a block diagram of an apparatus generating an error flag, according to an embodiment of the present invention. Referring to FIG. 3, the error flag generation apparatus includes a frame synchronization (frame-sync) detector 110, a memory 120, a frame synchronization (frame-sync) error memory 130, an error correction code decoder 140, an error flag generation unit 150, and a BIS (Burst Indicator Subcode) error flag memory 160.

[0018] The frame-sync detector 110 receives a reproduced digital signal, and outputs frame-sync error information indicating an error existence/absence for frame-sync data of frames forming a data block, to the frame-sync error memory 130. The frame-sync detector 110 also outputs a symbol signal for error correction to the memory 120. The digital signal input to the frame-sync detector 110 is a signal read from information stored in a disk (not shown) using an optical head (not shown), subjected to a high-frequency signal processing and equalizing, and reproduced.

[0019] FIGS. 4A- 4C are timing charts describing the generation of a frame-sync error signal by the frame-sync detector 110.

[0020] The frame-sync detector 110 generates a pseudo sync signal, shown in FIG. 4B coinciding with a frame-sync signal existing in an original digital signal. The frame-sync detector 110 compares the generated pseudo sync signal with a frame-sync signal of the reproduced digital signal, shown in FIG. 4C, and generates a frame-sync error signal, shown in FIG. 4A.

[0021] The memory 120 receives and stores the symbol signal for error correction transmitted from the frame-sync detector 110. The memory 120 stores the symbol signals with the error correction code format as shown in FIGS. 1 and 2 for each data block.

[0022] The frame-sync error memory 130 receives and stores the frame-sync error information transmitted from the frame-sync detector 110.

[0023] FIG. 5 is a view showing the structure of the frame-sync error memory 130. Referring to FIG. 5, the frame-sync error memory 130 has first through N-th frame-sync error memories each having the size of 1 x 496 bits and being capable of storing information of 496 bits indicating an error existence/absence for each of the 496 sync data included in one data block. Accordingly, frame-sync error information for one data block is stored in a frame-sync error memory with the size of 1 x 496 bits. N frame-sync error memories each having the size of 1 x 496 bits are provided to store frame-sync error information of N data blocks, considering the timing between the generation of a BIS error flag by the error correction code decoder 140 and the storage of the BIS error flag by the BIS error flag memory 160. According to an embodiment of the present invention, N is three.

[0024] The error correction code decoder 140 performs error-correction for BIS of the data block stored in the memory 120. Then, the error-correction code decoder 140 outputs a BIS error flag as information indicating an error existence/absence for each symbol of BIS to the error flag generator 150. The error flag generator 150 outputs the BIS error flag to the BIS error flag memory 160.

[0025] Thereafter, the error correction code decoder 140 receives an error flag generated by the error flag generator 150 and performs erasure correction for the symbol signal stored in the memory 120 for each data block.

[0026] The error flag generator 150 generates an error flag for erasure correction using the frame-sync error information stored in the frame-sync error memory 130 and the BIS error flag stored in the BIS error flag memory 160, and outputs the error flag to the error correction code decoder 140.

[0027] Referring to FIG. 2, the error flag generation operation of the error flag generator 150 will be described in detail. As shown in FIG. 2, one data frame includes four ECC data, each being 38 bytes wherein each ECC data is located between frame-sync data and BIS data or between BIS data and BIS data.

[0028] If both frame-sync error information and a BIS error flag of the frame-sync data and the BIS data which are neighboring a corresponding 38-byte ECC data, or both BIS error flags of BIS data which are neighboring a corresponding 38-byte ECC data indicate error existence, the error flag generator 150 generates an error flag requiring erasure correction for the

corresponding 38-byte ECC data, with reference to error information stored in the frame-sync error memory 130 and the BIS error flag memory 160.

[0029] The BIS error flag memory 160 receives the BIS error flag generated by the error correction decoder 140 via the error flag generator 150 and stores the received BIS error flag.

[0030] FIG. 6 is a view showing the structure of the BIS error flag memory 160. Referring to FIG. 6, one data block includes three BIS columns, with each BIS being 1 byte wherein each BIS column has 496 rows. Therefore, the BIS error flag memory 160 has first and M-th BIS error memories each being 1×496 bits and being capable of storing information of 496 bits indicating an error existence/absence for each BIS data included in one data block. According to an embodiment of the present invention, M is three.

[0031] Hereinafter, an error flag generation method according to the present invention will be described in detail.

[0032] FIG. 7 is a flowchart illustrating an error flag generation method according to an embodiment of the present invention.

[0033] The frame-sync detector 110 receives a reproduced digital signal for each data block (operation 210).

[0034] The frame-sync detector 110 generates frame-sync error information indicating an error existence/absence for the frame-sync data of each of the frames having a data block, and outputs the frame-sync error information to the frame-sync error memory 130 (operation 220). Also, the frame-sync detector 110 outputs a digital signal for error correction to the memory 120 for each data block.

[0035] The frame-sync error memory 130 receives the frame-sync error information corresponding to one data block from the frame-sync detector 110 and stores the received frame-sync error information (operation 230).

[0036] The frame-sync error memory 130 has first through N-th frame-sync error memories each being the size of 1×496 bits and being capable of storing information of 496 bits indicating an error existence/absence for the 496 sync data included in one data block. According to an embodiment of the present invention, N is three. Meanwhile, N frame-sync

error memories each having the size of 1 x 496 bits are provided to store the frame-sync error information of three data blocks, considering the timing between the generation of the BIS error flag by the error correction code decoder 140 and the storage of the BIS error flag by the BIS error flag memory 160.

[0037] The error correction code decoder 140 performs error-correction for BIS of the data block stored in the memory 120 and generates a BIS error flag as information indicating error existence/absence for each symbol of BIS (operation 240).

[0038] The error correction code decoder 140 outputs the generated BIS error flag to the error flag generator 150. The error flag generator 150 outputs the BIS error flag to the BIS error flag memory 160 and the BIS error flag memory 160 stores the BIS error flag (operation 250). The BIS error flag memory 160 has first through M-th BIS error memories each being the size of 1 x 496 bits and being capable of storing information of 496 bits, in order to indicate an error existence/absence for each BIS data included in one data block. According to an embodiment of the present invention, M is three.

[0039] The error flag generator 150 generates an error flag for erasure correction using the frame-sync error information stored in the frame-sync error memory 130 and the BIS error flag stored in the BIS error flag memory 160 (operation 260).

[0040] The error flag generator 150 generates an error flag requiring erasure correction of corresponding 38-byte ECC data, with reference to error information stored in the frame-sync error memory 130 and the BIS error flag memory 160, if both frame-sync error information of frame-sync data and a BIS error flag of BIS data which are neighboring a corresponding 38-byte ECC data, or both BIS error flags of BIS data which are neighboring a corresponding 38-byte ECC data indicate error existence.

[0041] The error correction code decoder 140 receives the error flag generated by the error flag generator 150 and performs erasure correction of the symbol signal stored in the memory 120 for each data block (operation 270).

[0042] As described above, the error flag generation apparatus and method for error correction, according to the present invention, can be easily implemented with improved error-correction performance and be advantageous in cost.

[0043] While the present invention has been particularly shown and described with reference to exemplary embodiments thereof, it will be understood by those of ordinary skill in the art that various changes in form and details may be made therein without departing from the spirit and scope of the present invention as defined by the following claims.